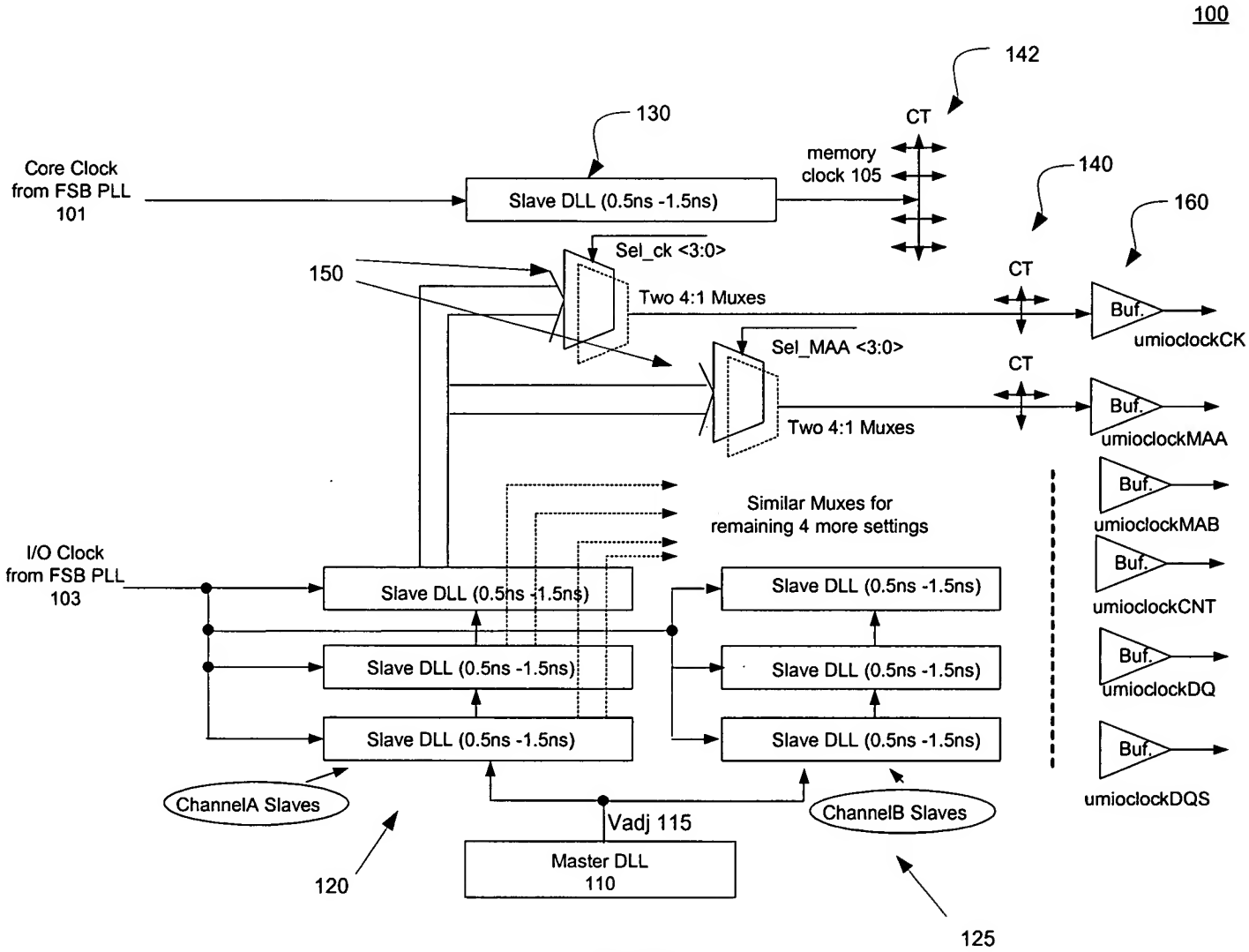
100
142
130
CT
memory
clock 105
Core Clock
from FSB PLL
101
Slave DLL (0.5ns -1.5ns)
140
160
Sel_ck <3:0>
150
CT
Two 4:1 Muxes
Buf.
umioclockCK
Sel_MAA <3:0>
CT
Buf.
Two 4:1 Muxes
umioclockMAA
Buf.
umioclockMAB
Similar Muxes for
remaining 4 more settings
Buf.
umioclockCNT
I/O Clock
from FSB PLL
103
Slave DLL (0.5ns -1.5ns)
Slave DLL (0.5ns -1.5ns)
Buf.
umioclockDQ
Slave DLL (0.5ns -1.5ns)
Slave DLL (0.5ns -1.5ns)
Slave DLL (0.5ns -1.5ns)
Slave DLL (0.5ns -1.5ns)
Buf.
umioclockDQS
ChannelA Slaves
ChannelB Slaves
Vadj 115
Master DLL
110
120
125

Figure 1

Slave Delay Lock Loop 200

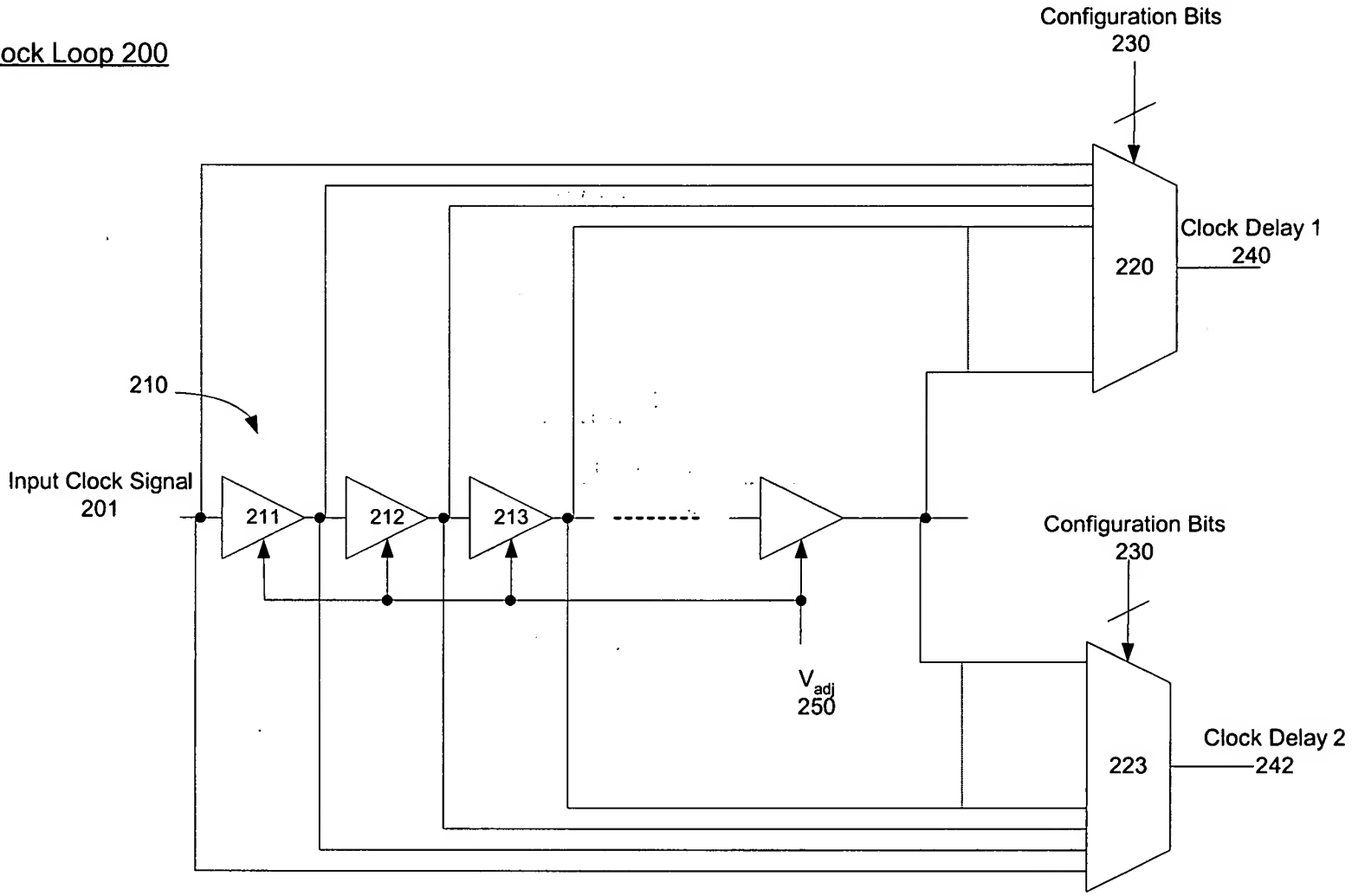

Figure 2A

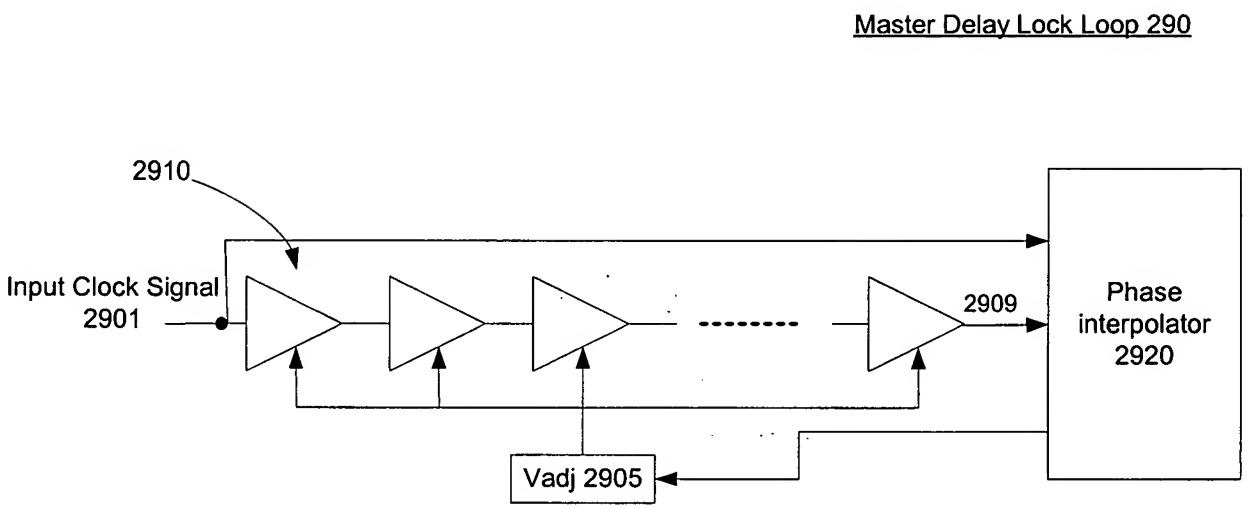
Master Delay Lock Loop 290
2910
Input Clock Signal
2901
2909
Phase
interpolator
2920
Vadj 2905

Figure 2B

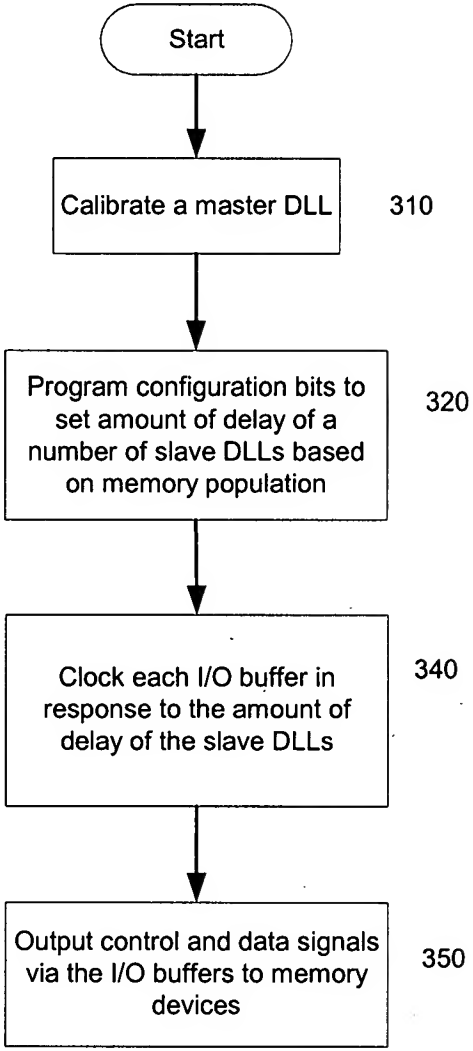
Start
Calibrate a master DLL
310
Program configuration bits to set amount of delay of a number of slave DLLs based on memory population
320
Clock each I/O buffer in response to the amount of delay of the slave DLLs
340
Output control and data signals via the I/O buffers to memory devices
350

Figure 3

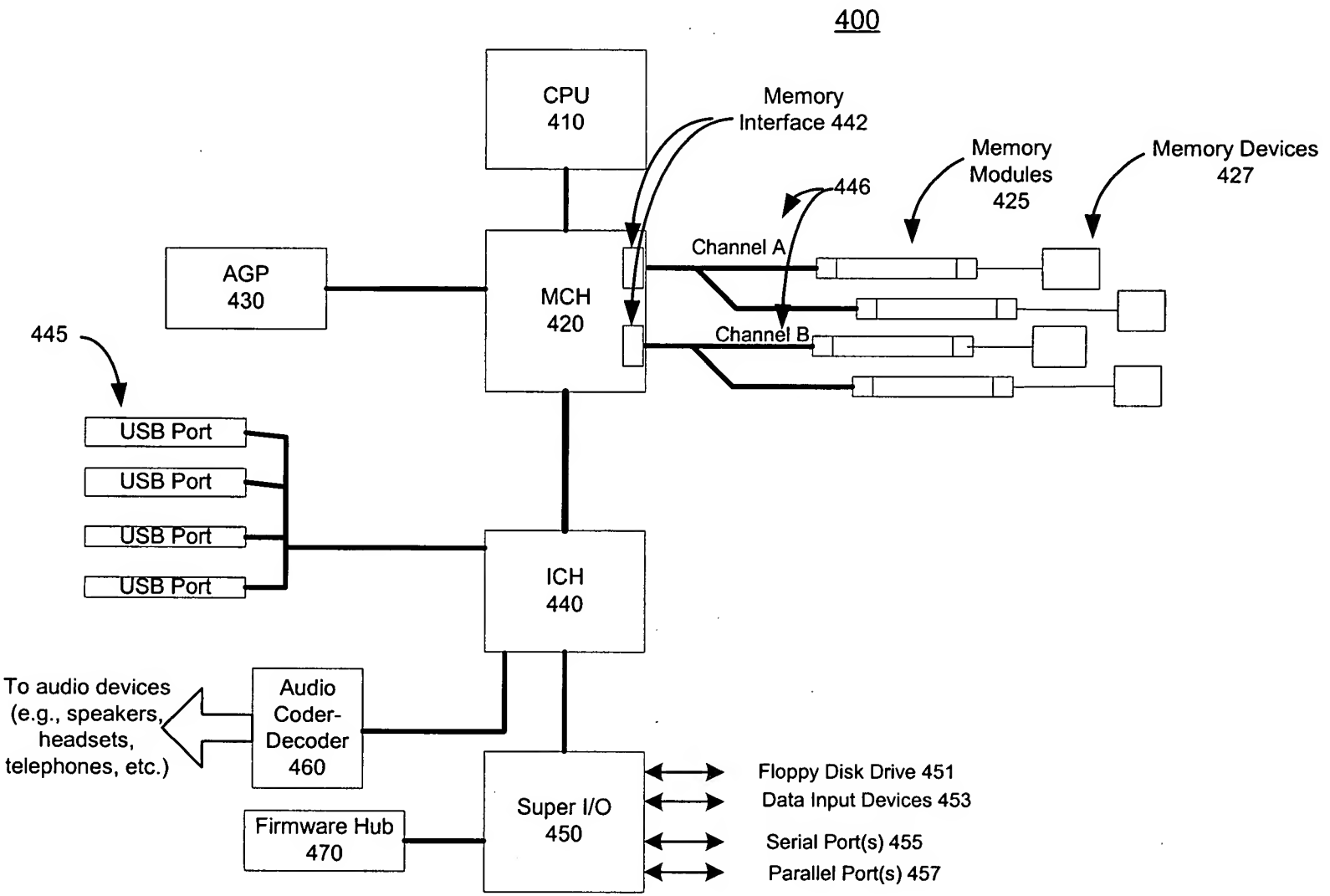
400
CPU
410
Memory
Interface 442
Memory
Modules
425
Memory Devices
427
446
AGP
430
MCH
420
Channel A
Channel B
445
USB Port
USB Port
USB Port
USB Port
ICH
440
To audio devices
(e.g., speakers,
headsets,
telephones, etc.)
Audio
Coder-
Decoder
460
Super I/O
450
Floppy Disk Drive 451
Data Input Devices 453
Serial Port(s) 455
Parallel Port(s) 457
Firmware Hub
470

Figure 4